How to use A1000 Testing Tool for Servicing

(WRAP AROUND TESTING JIG)

This manual is described as testing manual for servicing returned from your dealers and/or customers for service, with simple check system. Use fully this tool for your servicing.

This manual has contents as shown below

1. Main purpose and Name of Tool
2. Connection Layout between Tool and A1000
3. Operation and Testing Mode
4. Testing Mode instruction
5. Turbo PCB Operation
6. Caution

1. Main purpose and Name of Tool

A) Wrap Around Main PCB

Command to A1000 CPU function which controlled LOMAX ROM(Cartridge Slot) and recieve its data and display to LED on Testing Main PCB.

B) Turbo PCB

Margin test for operation clock.
Note; On connector J3, only clock uses. RGB signal passes.

C) Cartridge Slot

Having lomax V2.6.2 lTest Program for Wrap Around Main PCB.

D) Cable Assy

For all connection cables between A1000 and Testing Tool for each terminals are inclouding except K/B cable.

Parallel Bus cable for J8 , Serial Bus cable for J6 , Mouse port cable for J11 and J12, External Drive cable for J7 and Internal drive cable J10 .

Should be used K/B cable on A1000 for as a K/B cable.

2. Connection layout between Tool and A1000

Connect each cable assy for each connector both Tool and A1000 following below shown **Fig. A.**

Note; Need analog RGB monitor and Speaker system(2 Speakers and stereo amplifier) and spakers and monitor display have to be separated enoughly (more than 50 cm) each others .

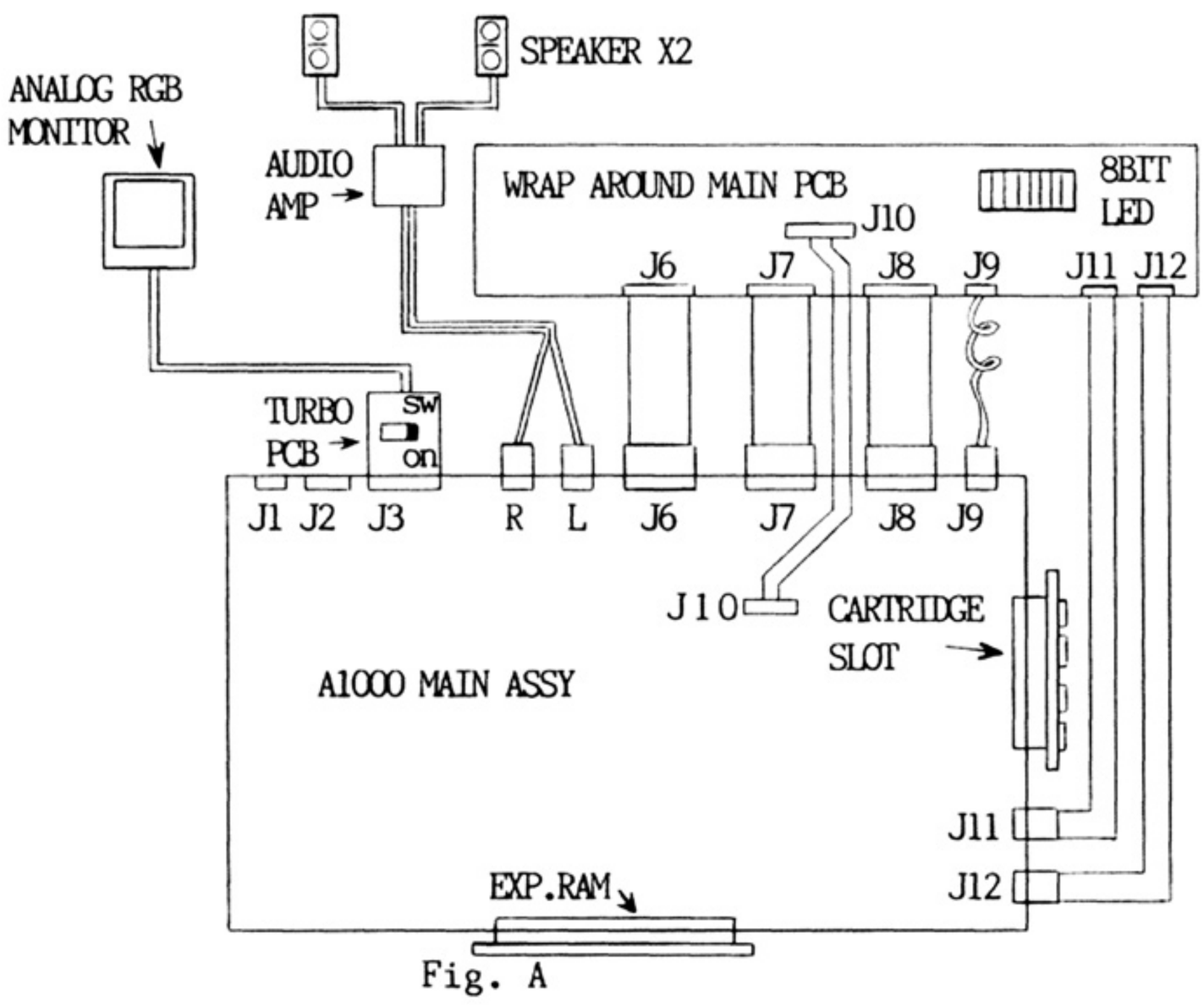

Fig. A

3. Operation and Testing Mode

A) Make sure connect followed Fig.A and Turbo SW Tune Off on initially.

B) After turning on A1000 power main SW, blinking LED signal will appear on Wrap Around main PCB. See screen and LED change process in **Fig. B**

C) Displaying white screen from black and sounding with in about 10 sec. The Centre of Sound will move right to left.

D) Colour of screen goes to black again after sound test completes

E) Screen will change to pattern I **(Fig.C)** in a few secs, after change to black.

F) Screen will change to Pattern II (**Fig.D**) after several sec. displaying Pattern I

G) Completes and test is Okay , if screen Pattern change I to II alternatively and it is repeated at intervals of several seconds.

H) When screen pattern does not appear and LED blinking stops, it is an error. Therefor, read the error code from LED and refer to the contents of error described in sheets 4—7.

Screen Display	LED (ON = □ OFF = ▨)
Black	□□□□□□□□
Black	▨□□□□▨▨
Black	Blinks
White	□▨▨▨▨□□
White	□▨▨▨▨▨□ *1
White	□□□▨▨▨▨□ *2
Black	□□□▨▨▨▨▨
Pattern I for 4sec. and then pattern II for 3sec. are repeated	▨▨▨▨▨▨▨□ Blinks one by one from right to left hereafter

Error code is indicated in hexadecimal digits.

Divide the 8-bit LED into 2 parts, left high order, right low order.
*1 Sound starts.
*2 Sound completes

Fig. B

Main defects :

1) Dotted vertical lines are seen in the 4096-color pattern.
2) Sprite blinks and the color is not clear enough.
3) White dots and lines are seen in the left corner of the red block, (first pixel error)

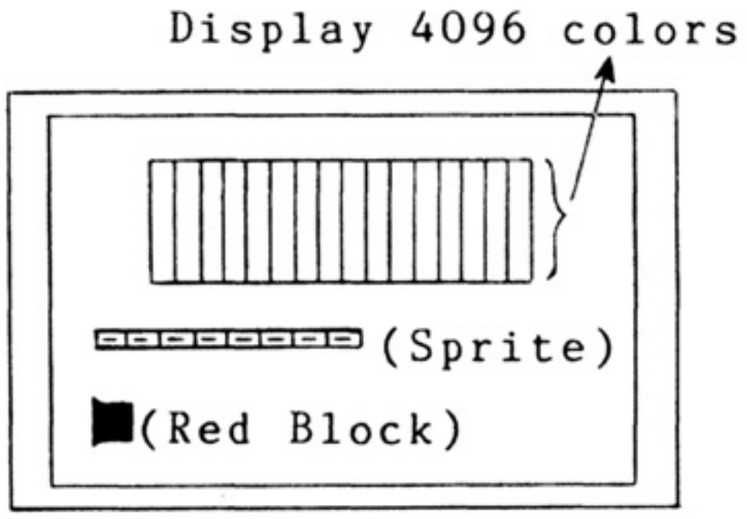

Fig.C Pattern I (Showham)

Main defects :

1) Dotted vertical lines are seen on the border line of glay-scale.
2) Color blurs in the color test pattern.

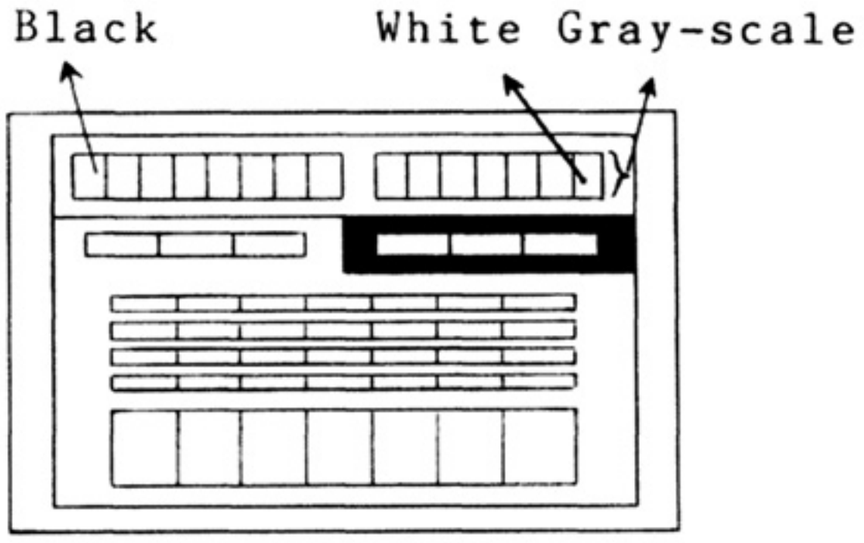

Fig.D Pattern II
(Color test pattern)

```
Test D   Write/Read a "J" character via the serial connection
Test F   Write/Read a "string" character via the serial connection
           Test U4E(U4F),pin 40 (transmit) . 41 (receive), U6K(U7N),pins 12/13,11 R38
           (R39),J6 pin  2 (transmit), U6l(U7P),  pins 8,10 R30(R30)  J6 pin 3
Test F   Keyboard Communication Test
            Tests U6P(U6I)  -pins 40 (kbd clock)  R8(R10)  J9 pin 2,J8 pin 12,U6P(U6T)
            pins 39 (kbd data)  R7(R9) J9 pin3,J8 pin 11
Test 10.  "SEL" line set as output,reset,except "CD"to be set
Test 11.  "SEL" line set as input, toggel and check "CD"     Test  U6N(U6S)-pin 4(SEL)
           J8 pin 13,    U6N(U6S)-pin 7(CD) J8 pin8,     U6L(U7P)-pins 6,4  R42(R43)
Test 20. Check parallel port Reset line,  s/b reset
Test 21.  Check Disk Port Reset line s/b reset
Test 22.  Check Serial Port Reset line,  s/b reset
Test 23.  Check Parallel Port Reset line can be set
lest 24.  Check Disk Port Reset line can be set
Test 25.  Check Serial Port Reset line can be set
            Parallel Port   U7H(U8P),  5/6  J8, pin 25,     Disk Port   U7R(U8T),5/6
           J7, pin 10,    Serial Port  U7NUJ8R), 13/12, J6, pin 25
Test 26.  Check Fire lines as output,  check if set
Test 27.  Check Fire lines as output,  check if cleared
```

4. Testing Mode instruction WRAP AROUND

Note; Observe proper RGB video

; The figure in parenthesis show the Location No. for 4 layer PCB.

Test 1. Check Ability to read last ROM location
Ihis is a general test of the processor and the 86-pin connector
Test 2. Set serial port as input, Test busy pout
Test U6N(U6S),pins 39,2-DAIA 40,3=CLOCK This is the CBM Serial BUS
Test 3. DRDY and ACK test
Tests U6P(U6T),pins 18(DRDY)and 24(ACK)
Test 4. Check the CBM Serial Bus
Test U6N(U6S)40,3=CLOCK 39,2-DATA
Test 5. Check RTS-CTS bit set loop
Test 6. Check RTS-CTS bit clear loop
Test 7. Check DTR-DSR bit set loop
Test 8. Check DTR-DSR bit clear loop
Test U6N(U6S) lines, U6K(U7l) and U6L(U7P) as follows;
RTS; U6N(U6S)-pin 8 U6K(U7L)-pin 2. 3 R 39(R40)J6 pin 4 ,
CTS; U6N(U6S)-pin 6 U6L(U7P)-pin 11,13 R 40(R41) J6 pin 5
DTR; U6N(U6S)-pin 9 U6K(U7L)-pin 4/5,6 R 31(R151)J6 pin 20
DSR; U6N(U6S)-pin 5 U61(U7P)-pin 3,1 R41(R42) J6 pin 6
Test 9. Roll a zero through the parallel port
Test A. Roll a one through the parallel port
Test U6P(U6I) ,pins 17-10 as bits 7-0 respectively J8pins 9-2

<LED NOW ARE ACTING>

Test B Write/Read a "?"character via the serial connection
Test C Write/Read an "E"character via the serial connection

Test 30. Verify keyboard +5 volts is Okay
Keyboard Connector,(J9) ,pin 1
Test 31. Verify Serial Port +5 volts is Okay
Serial Connector, (J6), pin 21
Test 32. Verify Joystick [1] +5 volts is Okay
Test 33. Verify Joystick [0] +5 volts is Okay
Left and Right joystick connectors, pin 7, Q9(Q8) and associated circuitry.
Test 34. Verify Disk Drive +5 volts is Okay J7 pin 12
Test 35. Check Keyboard Ground Keyboard connector, J9, pin 4
Test 36. Check Internal Disk Ground Internal Disk Connector, J10, pin 25
Test 37. Check External Disk Ground External Disk Connector, J7, pin 7
Test 38. Check Serial Port Ground number 2 Serial Connector, J6, pin 7
Test 39. Check Serial Port Ground number 1 Serial Connector, J6, pin 1
Test 3A. Check Joystick [1] Ground
Test 3B. Check Joystick [0] Ground J12, pin 8 J 11, pin 8
Test 40. Test Short Circuit Protection (SCP) on Joystick [1] Power Q9(Q8) and associated circuitry
Test 45. Clear Short, check that Joystick [1] power was restored Q9(Q8) and associated circuitry
Test 47. Table Drive Joystick Position Checking

J12, pin 1 FORWARD	U1M(U1T) pin 3	Note;	Test 47 failures are
J12, pin 2 BACK	U1H(U1T) pin 13		offen caused by D-ram
J12, pin 3 LEU	U1H(U1l)pin 2		failed. Please check video
J12, pin 4 RIGHT	U1H(U1f) pin 14		display for Correct image.
J11, pin 1 FORWARD	U1M(U1T) pin 10		If image is wrong, D-ram
J11, pin 3 LEFT	U1H(U1f) pin 11		is probably bad
J12, FORWARD/LEFT 4	U1M(U1I) pin 39	J11, pin 4 RIGHT	U4A(U4A) pin 5
J11, FORWARD/LEFT 9	U1M(U1I) pin 38	J12, BACK/RIGHT 12	U4A(U4A) pin 8
J11, pin 2 BACK	U1H(U1I) pin 6	J11, BACK/RIGHT 7	U4A(U4A) pin 9

Test 50. Set all Pot lines to output(pull down), Verify all L
Test 51. Toggle Pot[X] Port[1], Verify line goes Hi
Test 52. Toggle Pot[Y] Port[1], Verify line goes Hi
Test 53. Toggle Pot[X] Port[0], Verify line goes Hi
Test 54. Toggle Pot[Y] Port[0], Verify line goes Hi
Test 55. Set all Pot lines to output(pull up), Verify all High
Test 56. Toggle Pot[X] Port[1], Verify line goes Lo
Test 57. Toggle Pot[Y] Port[1], Verify line goes Lo
Test 58. Toggle Pot[X] Port[0], Verify line goes lo
Test 59. Joggle Pot[Y] Port[0], Verify line goes Lo
Test 5A. Set up to Begin testing the Pots as input
Test 5B. Pot Input load testing on all
Test 5C. Pot Input load testing on Pot X Port 1

Test 5D. Pot Input load testing on Pot Y Port 1
Test 5E. Pot Input load testing on Pot X Port 0
Test 5F. Pot Input load testing on Pot Y Port 0
Pot X, Port 0; R122 C120 U4L (U4F) pin, 32 J12, pin 5
Pot Y, Port 0; R121 C119 IMF (Ü4F) pin. 33 J12, pin 9
Pot X, Port 1; R115 C121 U4F (U4F) pin, 35 J11. pin 5
Pot Y, Port 1; R114 C122 U4E (U4F) pin, 36 J11, pin 9
Test 60. Test External Disk Control lines
/SEL1B J7, pin 21 U6N(U68),pin 14 * /SEL3B J7. pin 20 U6N, pin 16 *
DIRB J7, pin 19 U6N, pin 11 * /STEPB J7, pin 18 U6N, pin 10 *
/DKWEB J7, pin 16 U6N, pin 39 * /SIDEB J7, pin 13 U6N, pin 12 *
/SEL2B J7, pin 9 U6N, pin 1b * /MTRXD J7, pin 8 U6N, pin 17 *
*; Please see schematic for intermediate pins
Test 6A. Test Internal Disk Control lines and Ground line
/SIDEB J10, pin 32 U6N(U6S),pin 12 * /DKWEB J10, pin 24 U6N, pin 39 *
/STEPB J10, pin 20 U6N, pin 10 * DIRB J10, pin 18 U6N, pin 11 *
/MTROD J10, pin 16,4 U6N, pin 17 * /SEL0B J10, pin 10 U6N, pin 13 *
Test 6B. Test Light Pen Function
Test 72. Test Disk RESPONCE line
/CHNG J7, pin 11 U6P(U6I), pin 4 * /WPRO J 7, pin 14 U6P. pin 5 *
/TKO J7, pin 15 U6P, pin 6 * /RDY J 7, pin 1 U6P, pin 7 *
Test 76. Test Disk Responce "INDEX" line
Test 77. Try to force a Reset Test with a "NARROW" pulse
Test the 2901 [U4M](U5M), and associated circuitry
Test 78. Memory Bit Checking
Test 79. Complimetary Bit Checking
Test 7A. Sliding ZEROs pattern
Test 7B. Sliding ONEs pattern
Test 7C. Address as DAIA Test
Test 7D. Inverted Address as DAIA Test
Test 7E. Bytefill Test
Test 80. ROM Checksum Checking
For the memory tests, there is not yet sufficient documentation generated
to allow troubleshooting down to the Chip level
Test 81/87. RAMROM memory ckeck
Test 83. Test ROM/RAM Strobe
Test 84. Test ROM/RAM Address lines
Test 85. Fest ROM/RAM Pattern
Test 88. WRITE protect on ROM/RAM
Test 89. Check Ihe Four Audio Channels, and audio DMA

Test 90. Custom Chip Resister Testing, Clear ADKCON
Test 91. Check ADKCON set and clear bit loop
Test 92. Custom Chip Resister testing, Clear CLXDAT
Test 93. Check DMACON[R] resister
Test 94. Check INTREQ resister
Test 95. Check INTENA resister
Test 96. Test JOYSTICK resister pattern #1
lest 97. Test JOYSTICK resister pattern #2
Test 98. Test JOYSTICK resister pattern #3
Test 99. Test JOYSTICK resister pattern #4

These are the change to the wraparound test description for loMax 2.3.2

1. Add the following 8 test items after "test A"

Test FO Check Ram Bus Bits 8,9,10,11 (U2C or U1C)
lest F1 Check Ram Bus Bits 12,13,14,15 (U2B or U1B)
Test F2 Check Ram Bus Bits 0,1.2,3 (U2F or U1T)
Test F3 Check Ram Bus Bits 4,5,6,7 (U2D or U10)
Test F4 Check Ram Bus Bits 8,9,10,11 (U1C)
Test F5 Check Ram Bus Bits 12,13,14,15 (U1B)
Test F6 Check Ram Bus Bits 0,1,2,3 (U1E)
Test F7 Check Ram Bus Bits 4,5,6,7 (U1D)

2. Remove tests 78 through 7E from the end of the document and put tests 78 through 7E here before "test B".

5. Turbo PCB Operation

Margine test which operation clock is 5% faster can be performed by the switch of the Turbo PCB on and proceed Wrap Around test.(Test items are as same as switch off) .
When operation clock become 5% faster,it will be impossible to synchronize the RGB monitor. In this case, adujst the Horizontal Hold variable resister inside the moniter to get normal picture.
(Original inside clock is 28.63636MHz and Turbo clock is around 30MHz.)

6. CAUTION

Though this Testing Jig can be used for both NTSC and PAL in common, use Rom's (ODD, EVEN) on cartridge PCB V 2.6.2 for NTSC AND V 2.6.2P for PAL.

This testing Jig has no protection such as enclosures. Be careful not to break IC's and other electronics components by short circuit or Static Electricity.